# Reversible $k$-valued logic circuits are finitely generated for odd $k$

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## 1 Introduction

Let $\mathbb{Z}_k = \{0, \ldots, k-1\}$, and let $\mathfrak{S}[k]$ be the monoidal groupoid whose objects are natural numbers $n$, and whose morphisms $f : k \to k$ are invertible functions $f : \mathbb{Z}_k^n \to \mathbb{Z}_k^n$. In his 2003 paper "Towards an algebraic theory of Boolean circuits" [1, p. 298], Lafont notes that, although $\mathfrak{S}[k]$ is not finitely generated when $k$ is even, it is finitely generated when $k$ is odd. For the proof, he cites a private communication by me. The purpose of this short note is to make the content of that unpublished communication available.

Since the proof referred to in Lafont's paper was never published, others have proved the result independently. The earliest such published proof that I am aware of is due to Boykett [2].

## 2 Background: linear and affine invertible functions

Let $\mathbf{GL}(\mathbb{Z}_k)$ and $\mathbf{GA}(\mathbb{Z}_k)$ be the monoidal subgroupoids of $\mathfrak{S}[k]$ consisting of invertible linear functions and invertible affine functions, respectively. Here, we regard $\mathbb{Z}_k$ as a ring with addition and multiplication. As usual, a function $f : \mathbb{Z}_k^n \to \mathbb{Z}_k^n$ is *linear* if $f(v + w) = f(v) + f(w)$ and $f(av) = af(v)$ for all $v, w \in \mathbb{Z}_k^n$ and $a \in \mathbb{Z}_k$, and $f$ is *affine* if there exists some $u \in \mathbb{Z}_k^n$ and a linear function $g$ such that $f(v) = u + g(v)$, for all $v$. It is well-known from the theory of integer matrices that $\mathbf{GL}(\mathbb{Z}_k)$ is finitely generated by the gates $D, U : 2 \to 2$, given by $D(x, y) = (x, x + y)$ and $U(x, y) = (x + y, y)$, together with a gate $H_a : 1 \to 1$ for each invertible element $a \in \mathbb{Z}_k$, given by $H_a(x) = ax$. If we moreover add a gate $v : 1 \to 1$ defined by $v(x) = x + 1$, we obtain a finite set of generators for $\mathbf{GA}(\mathbb{Z}_k)$. Lafont's notation for these gates is shown in Figure 1.

Note that the single transposition $(0, \ldots, 0, 0) \leftrightarrow (0, \ldots, 0, 1)$ of $\mathbb{Z}_k^n$, together with all invertible affine transformations, suffices to generate the group of invertible functions on $\mathbb{Z}_k^n$. This is because by taking affine conjugates, we can get all transpositions of the form $(x_1, x_2, \ldots, x_{k-1}, x_k, x_{k+1}, \ldots, x_n) \leftrightarrow (x_1, x_2, \ldots, x_{k-1}, x_k + 1, x_{k+1}, \ldots, x_n)$. These generate all invertible functions because the permutation group $S(X)$ on any set $X$ is generated by any set of transpositions $(ab)$ that form the edges of a connected graph on $X$.

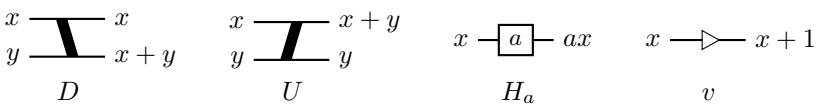


Figure 1: Affine gates

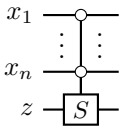


Figure 2: The controlled negation gate $S_{n+1}$

# 3 The result

**Proposition 1.** *If $k \geqslant 3$ is odd, then $\mathfrak{S}[k]$ is finitely generated. In fact, it is generated by gates of arity 2 and less.*

*Proof.* Let $S : 1 \to 1$ be the "generalized negation" gate defined by $S(0) = 1$, $S(1) = 0$, and $S(x) = x$ otherwise. Consider the "controlled negation" gate, defined by

$$S_{n+1}(x_1, \ldots, x_n, z) = (x_1, \ldots, x_n, z'),$$

where $z' = S(z)$ if $x_1, \ldots, x_n = 0$, and $z' = z$ otherwise. Figure 2 shows the notation we use for the controlled negation gate. The gate $S_n$ corresponds to a single transposition of $\mathbb{Z}_k^n$, exchanging $(0, \ldots, 0, 0)$ and $(0, \ldots, 0, 1)$. Therefore, the family of gates $S_n$ for $n \geqslant 1$, together with the affine transformations, generates $\mathfrak{S}[k]$.

Now consider the circuits $T$ and $U$ defined in Figure 3. This circuit $T$ performs two transpositions $(0, 0, 0) \leftrightarrow (0, 0, 1)$ and $(0, 1, 0) \leftrightarrow (0, 1, 1)$ and is the identity elsewhere. The circuit $U$ uses $(k-1)/2$ affine conjugates of $T$ to perform the $k-1$ transpositions $(0, x, 0) \leftrightarrow (0, x, 1)$, for $x = 1, \ldots, k-1$, and is the identity elsewhere.

Finally, if we compose $U$ with $S_2$ as shown in Figure 4, we obtain a single transposition $(0, 0, 0) \leftrightarrow (0, 0, 1)$, or in other words, $S_3$. Therefore, $S_3$ is definable from $S_2$ in the presence of affine gates. By adding $n$ additional controls to every $S$-gate, it follows that $S_{n+3}$ is definable from $S_{n+2}$, for all $n \geqslant 0$. By induction, all $S_n$ for $n \geqslant 3$ are definable from $S_2$, and therefore $\mathfrak{S}[k]$ is finitely generated when $k$ is odd and $k \geqslant 3$. □

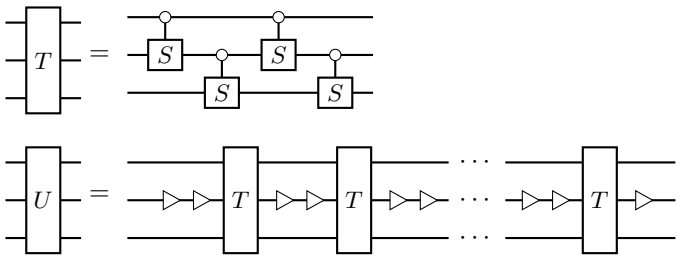


Figure 3: The circuits $T$ and $U$. Here, $U$ contains $\frac{k-1}{2}$ occurrences of $T$ and $k$ occurrences of the affine $v$-gate.

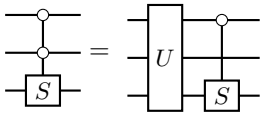


Figure 4: Expressing $S_3$ in terms of $S_2$ and affine gates

# References

[1] Yves Lafont. Towards an algebraic theory of Boolean circuits. *Journal of Pure and Applied Algebra*, 184:257–310, 2003.

[2] Tim Boykett. Closed systems of invertible maps. Available from `arXiv:1512.06813`, 2015.